CLAIMS

1. A complementary bipolar semiconductor device, hereinafter referred to as a CBi semiconductor device,

- comprising a substrate of a first conductivity type and a number of active regions which are provided thereon and which are delimited in the lateral direction by shallow field insulation regions,

- in which vertical npn-bipolar transistors with an epitaxial base are arranged in a first subnumber of the active bipolar transistor regions and vertical pnp-bipolar transistors with an epitaxial base are arranged in a second subnumber of the active bipolar transistor regions,

- wherein either one transistor type or both transistor types have both a collector region and also a collector contact region in one and the same respective active bipolar transistor region,

characterised in that in a first transistor type in which the conductivity type of the substrate is identical to that of the collector region an insulation doping region is provided between the collector region and the substrate, the insulation doping region being adapted to provide electrical insulation of the collector and the substrate,

wherein in the region of an interface between the collector region and the insulation doping region there is a p-n junction which is arranged no deeper at the edge defined by the field insulation region of the active bipolar transistor region in question, alternatively in the whole of the respective active bipolar transistor region, than the lower edge of the shallow field insulation regions, and

the collector region either of the first transistor type or both transistor types is delimited laterally by the shallow field insulation regions.

2. A CBi semiconductor device as set forth in one of the preceding claims in which the dopant concentration of the insulation doping in the space charge region near the collector is less than 1×10^{17} cm^{-3}.

3. A CBi semiconductor device as set forth in one of the preceding claims in which the dopant concentration of the insulation doping in the space charge region near the collector is at a maximum 1×10^{16} cm^{-3}.

4. A CBi semiconductor device as set forth in one of the preceding claims in which the dopant concentration of the insulation doping in the space charge region near the collector is less than 1×10^{15} cm^{-3}.

5. A CBi semiconductor device as set forth in one of the preceding claims in which in the first transistor type in a laterally adjacent active region there are provided a well of the second conductivity type opposite to the first conductivity type and a contact region associated therewith of the second conductivity type.

6. A CBi semiconductor device as set forth in one of the preceding claims in which the dopant dose of the well (4) is between 5×10^{12} cm^{-2} and 5×10^{14} cm^{-2}.

7. A CBi semiconductor device as set forth in one of the preceding claims in which the dopant dose of the well is restrictedly between 1×10^{13} cm^{-2} and 2×10^{14} cm^{-2}.

8. A CBi semiconductor device as set forth in one of claims 5 through 7 in which the well is a well produced in an MOS process of the second conductivity type.

9. A CBi semiconductor device as set forth in one of the preceding claims in which the dopant concentration of the contact region is between 1×10^{17} cm^{-3} and 1×10^{21} cm^{-3}.

10. A CBi semiconductor device as set forth in one of the preceding claims in which the well and the substrate contact region laterally surround

the insulation doping region at two, alternatively three, alternatively four sides.

11. A CBi semiconductor device as set forth in one of the preceding claims in which the maximum dopant concentration in the collector contact region of the first or second transistor type is between 1×10^{18} cm^{-3} and 5×10^{20} cm^{-3}.

12. A CBi semiconductor device as set forth in one of the preceding claims in which the first or the second transistor type or both transistor types have an inner base region, below which is arranged a second collector region of either the same or approximately the same lateral extent as the inner base region, which second collector region with the same conductivity type is more highly doped than at least one portion, adjoining the second collector region, of the collector region.

13. A CBi semiconductor device as set forth in one of the preceding claims in which the epitaxial base includes a base layer stack with a plurality of layers which are monocrystalline in the inner base region and polycrystalline in portions which in the lateral direction are outside the inner base region and are referred to hereinafter as the base contact region.

14. A CBi semiconductor device as set forth in one of the preceding claims in which the base layer stack contains a base layer which is made either from silicon or from silicon-germanium and which is of a thickness of between 1 and 100 nm, in particular between 1 and 35 nm.

15. A CBi semiconductor device as set forth in one of the preceding claims in which the base layer stack includes a cover layer adjoining the base layer at the emitter side.

16. A CBi semiconductor device as set forth in one of the preceding claims in which one or more of the layers of the base layer stack are doped with carbon.

17. A CBi semiconductor device as set forth in one of the preceding claims in which an emitter either of the first or the second or both transistor types is of a T-shaped configuration.

18. A CBi semiconductor device as set forth in one of the preceding claims in which a substrate-side portion of the base contact region, which portion is provided in the base layer stack of the first transistor type, is made from the same, simultaneously deposited polycrystalline semiconductor material as a base-side outer portion of the transverse bar of the T-shape of the emitter in the second transistor type.

19. A CBi semiconductor device as set forth in one of the preceding claims in which an emitter-side vertical layer portion of the base contact region, which layer portion is provided in the base layer stack of the first transistor type, is made from the same simultaneously deposited polycrystalline semiconductor material as a contact-side vertical layer portion of the transverse bar of the T-shape of the emitter in the second transistor type.

20. A CBi semiconductor device as set forth in one of the preceding claims in which

- in the first transistor type the polycrystalline base contact region in the base layer stack has an interface which extends in parallel relationship with the substrate surface and along which grain boundaries of here mutually adjoining base-side and emitter-side, polycrystalline, vertical layer portions are oriented, and

- in the second transistor type the emitter has an interface which extends parallel to the substrate surface and along which grain boundaries

of here mutually adjoining base-side and contact-side, polycrystalline, vertical layer portions are oriented.

21. A CBi semiconductor device as set forth in one of the preceding claims in which the shallow field insulation regions are in the form of shallow trenches.

22. A CBiMOS or CBiCMOS semiconductor device as set forth in one of the preceding claims with additionally at least one MOS semiconductor component or with complementary MOS semiconductor components.

23. A CBi or CBiMOS or CBiCMOS semiconductor device as set forth in one of the preceding claims in which the substrate is p-conducting and the first transistor type is a pnp-transistor and the second transistor type is an npn-transistor.

24. A process for the production of complementary, high frequency-suited bipolar transistors in a semiconductor device as set forth in one of claims 1 through 23

- in which the layers of both bipolar transistor types are deposited on active bipolar transistor regions of a substrate of a first conductivity type, which is pre-structured by shallow field insulation regions, and structured,
- in which in one or both bipolar transistor types a collector region and a collector contact region are produced within one and the same active bipolar transistor region,
- in which in that bipolar transistor type whose collector region is of the same conductivity type as the substrate an insulation doping region is produced beneath the collector region in an implantation step in such a way that the collector region is electrically insulated from the substrate, and
- in which the implantation step is carried out in such a way that in the region of an interface between the collector region and the insulation doping region there is produced a pn-junction which at the edge, defined by the field insulation regions, of the active bipolar transistor region in

question, alternatively in the entire respective active bipolar transistor region, is arranged no deeper than the lower edge of the shallow field insulation regions.

25. A process as set forth in claim 24 in which during the implantation step to produce the collector region a second implantation step is carried out for at least partial amorphisation of the collector region.

26. A process as set forth in claim 25 in which after the second implantation step a step for recrystallisation of the collector region is carried out.

27. A process as set forth in one of claims 24 through 26 in which a substrate-side layer portion of the base contact region, said layer portion being provided in the base layer stack of the first transistor type, is deposited simultaneously with a base-side layer portion of the transverse bar of the T-shape of the emitter in the second transistor type.

28. A process as set forth in one of claims 24 through 27 in which an emitter-side layer portion of the base contact region, said layer portion being provided in the base layer stack of the first transistor type, is deposited simultaneously with a contact-side layer portion of the transverse bar of the T-shape of the emitter in the second transistor type.

29. A process as set forth in one of claims 24 through 28 in which the bipolar process module is carried out in the context of the CMOS process following a gate structuring operation and an operation for the formation of gate spacers and prior to the implantation of source and drain regions.

30. A process as set forth in one of claims 24 through 29 in which the bipolar transistors are produced on an SOI substrate.

31. A process as set forth in claim 30 in which the bipolar transistors are produced on an SOI substrate with a thin Si cover layer of less than 50 nm layer thickness.

32. A process for the production of a CBiMOS or CBiCMOS semiconductor device characterised by a process module integrated into the process, with the steps of the process as set forth in one of claims 24 through 31.